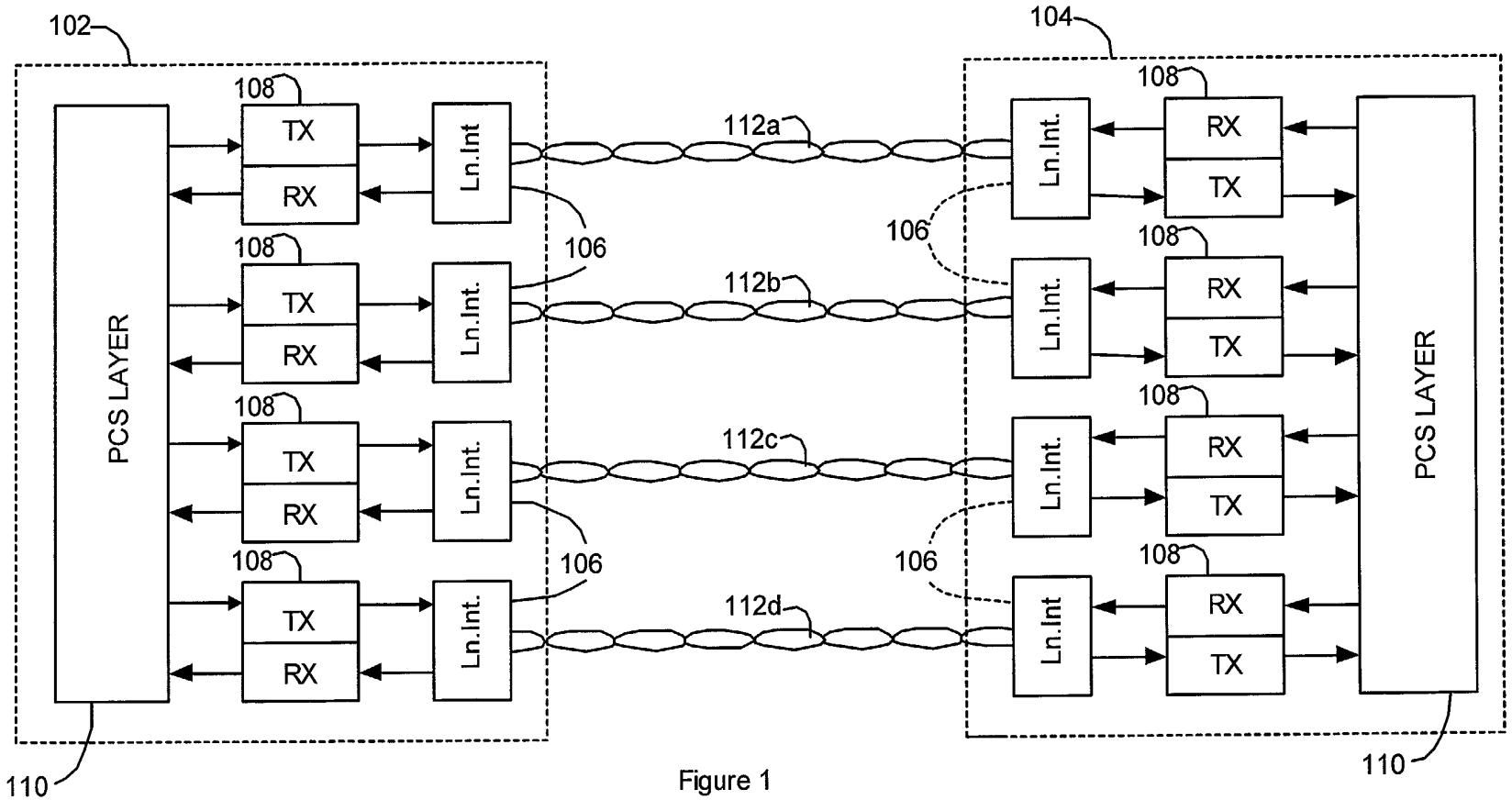


Figure 1

20050052798001

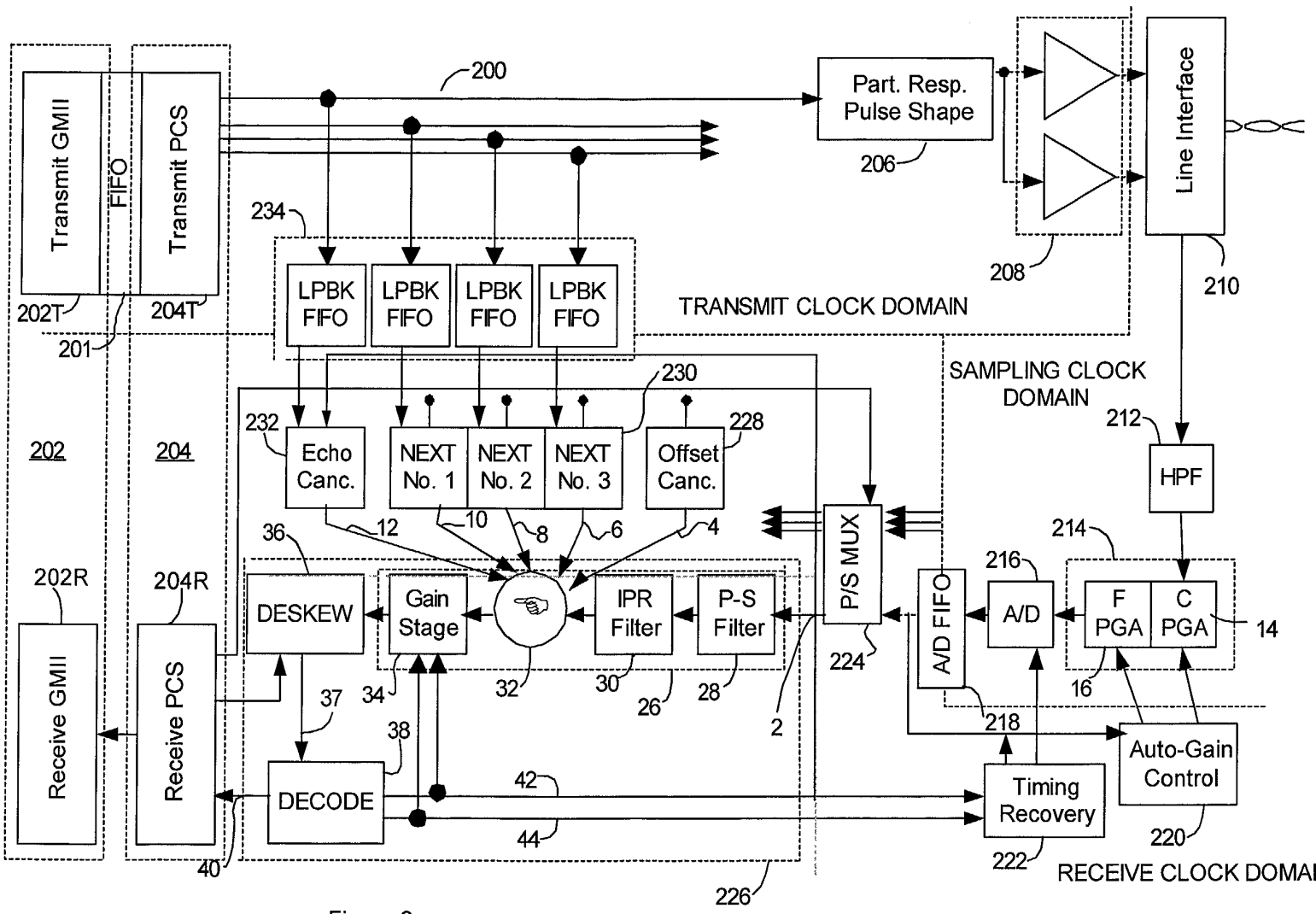


Figure 2

20100927 "S2798001"

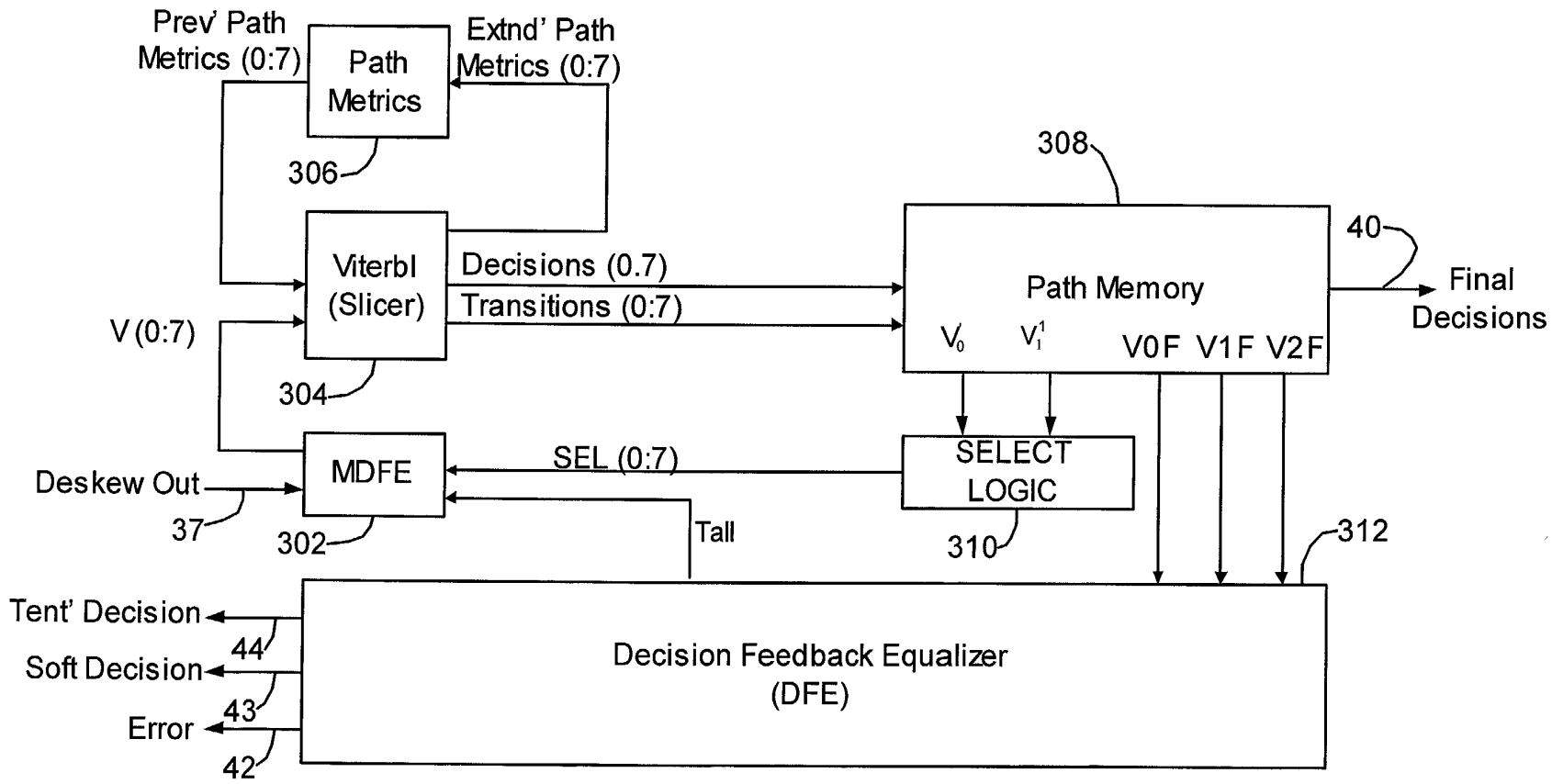


Figure 3

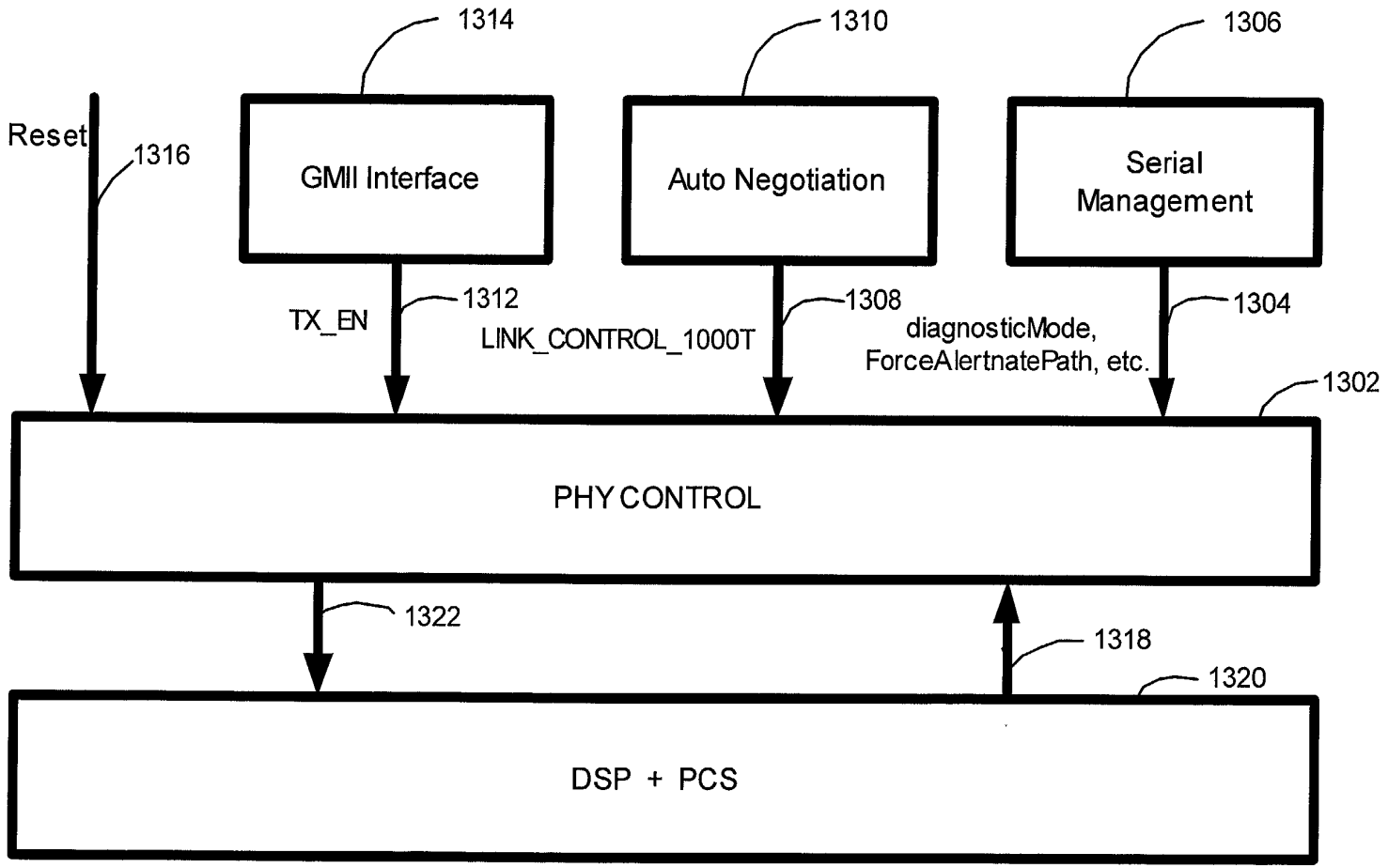

1314
1310
1306
Reset
1316
GMII Interface
Auto Negotiation
Serial Management
TX_EN
1312
LINK_CONTROL_1000T
1308
diagnosticMode,
ForceAlertnatePath, etc.
1304
1302
PHY CONTROL
1322
1318
1320
DSP + PCS

FIG. 4

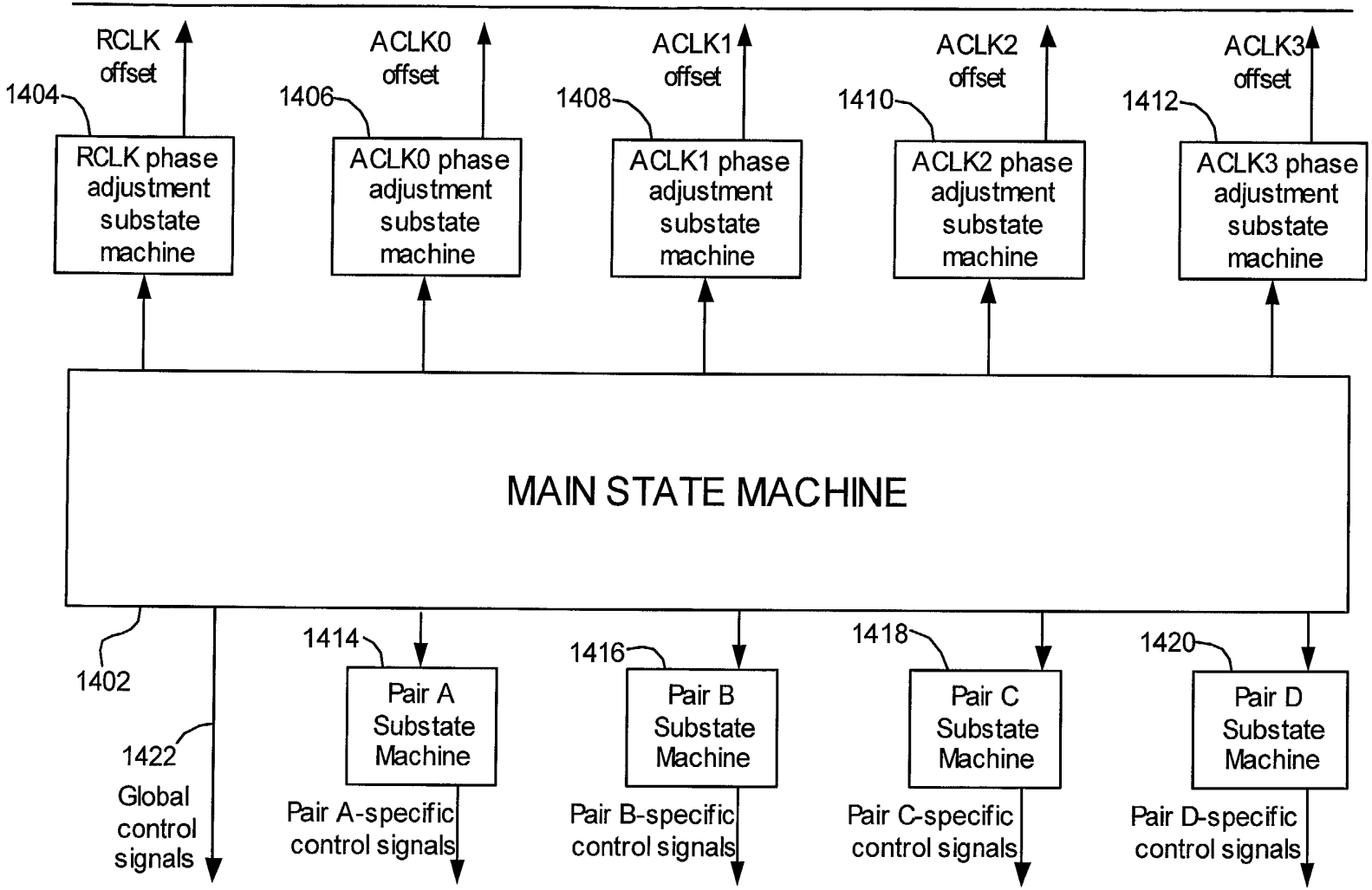

RCLK offset
ACLK0 offset
ACLK1 offset
ACLK2 offset
ACLK3 offset
1404
1406
1408
1410
1412
RCLK phase adjustment substate machine
ACLK0 phase adjustment substate machine
ACLK1 phase adjustment substate machine
ACLK2 phase adjustment substate machine
ACLK3 phase adjustment substate machine
MAIN STATE MACHINE
1402
1422
Global control signals
1414
Pair A Substate Machine
Pair A-specific control signals
1416
Pair B Substate Machine
Pair B-specific control signals
1418
Pair C Substate Machine
Pair C-specific control signals
1420
Pair D Substate Machine
Pair D-specific control signals

Figure 5

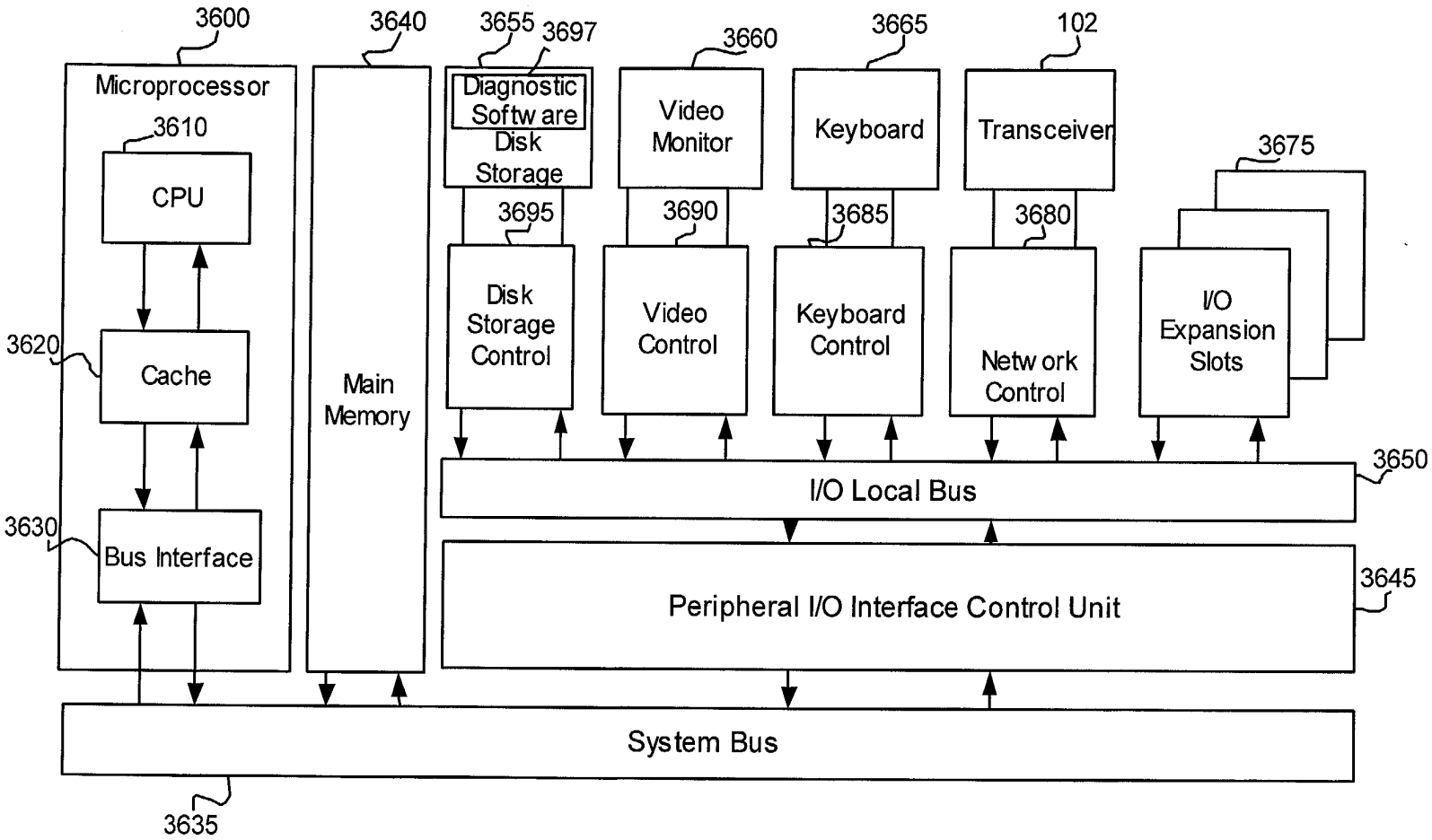

3600
Microprocessor
3610
CPU
3620
Cache
3630
Bus Interface
3640
Main Memory
3655
3697
Diagnostic Softw are
Disk Storage
3695
Disk Storage Control
3660
Video Monitor
3690
Video Control
3665
Keyboard
3685
Keyboard Control
102
Transceiver
3680
Netw ork Control
3675
I/O Expansion Slots
3650
I/O Local Bus
3645
Peripheral I/O Interface Control Unit
System Bus
3635

Figure 6

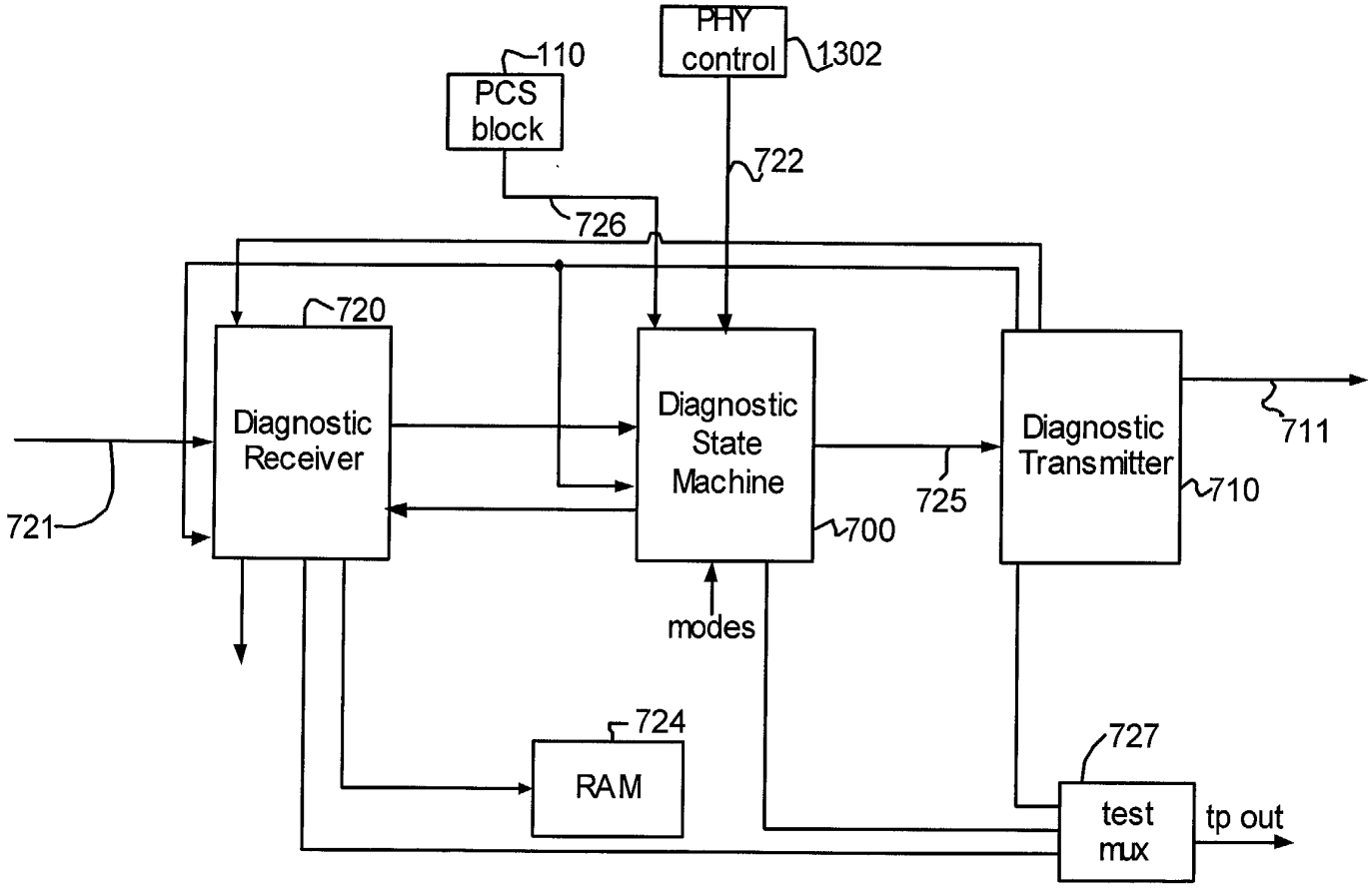

PHY control
1302
110
PCS block
722
726
720
Diagnostic Receiver
Diagnostic State Machine
Diagnostic Transmitter
711
721
725
710
700
modes
724
RAM
727
test mux
tp out

Figure 7

Master - no FEXT

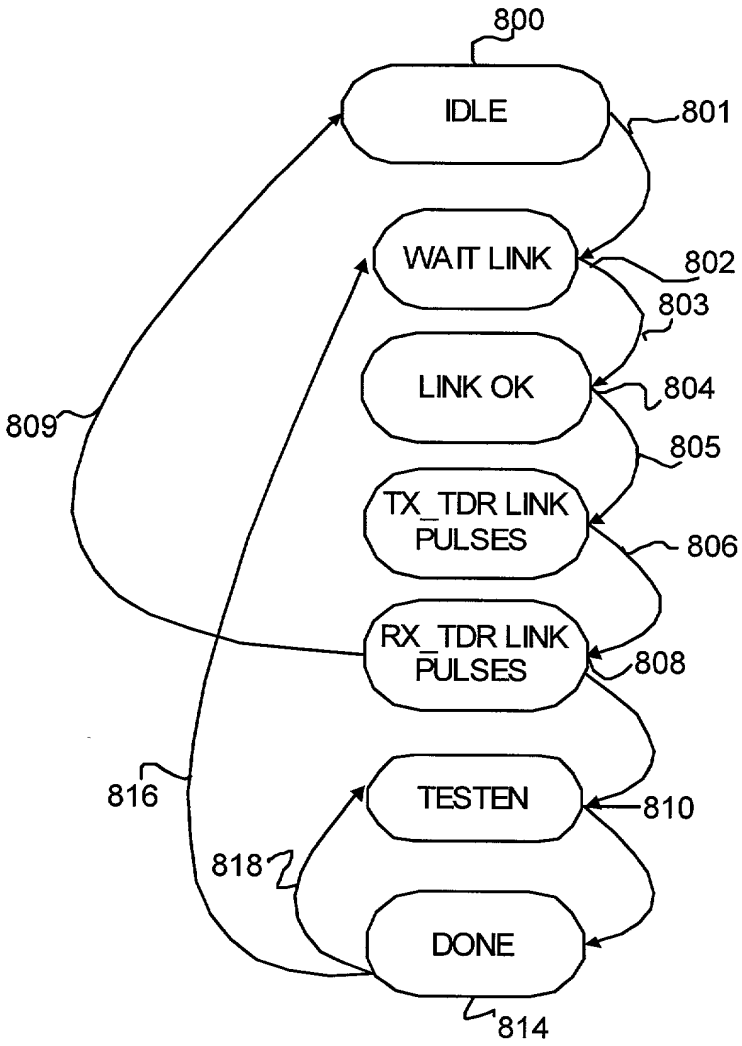


Figure 8

slave - no FEXT

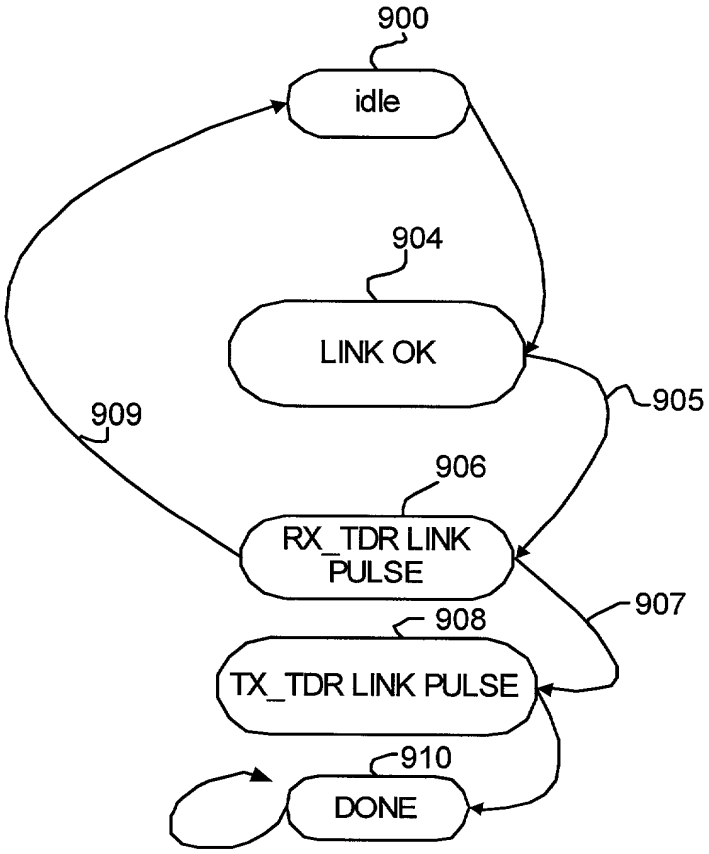


Figure 9

Echo/Next - no extphy

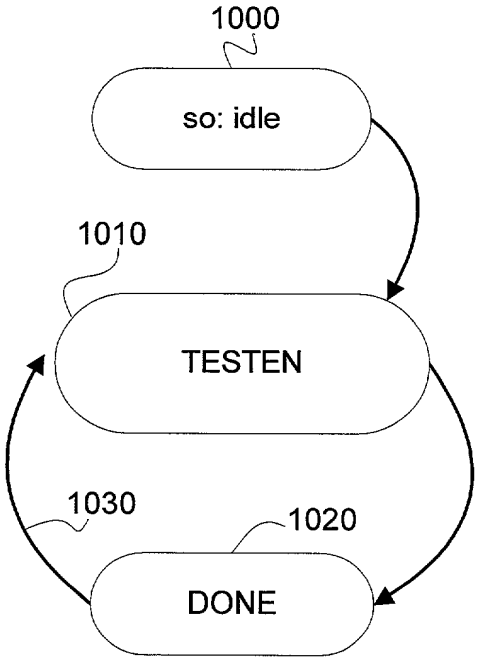


Figure 10

Master - FEXT

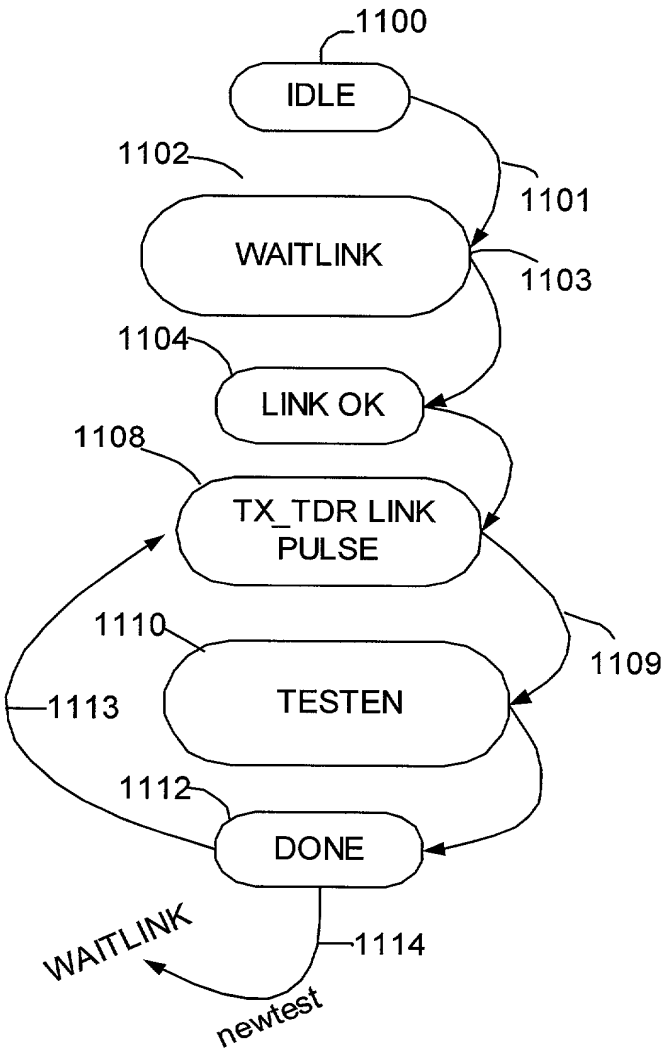


Figure 11

Slave- fext

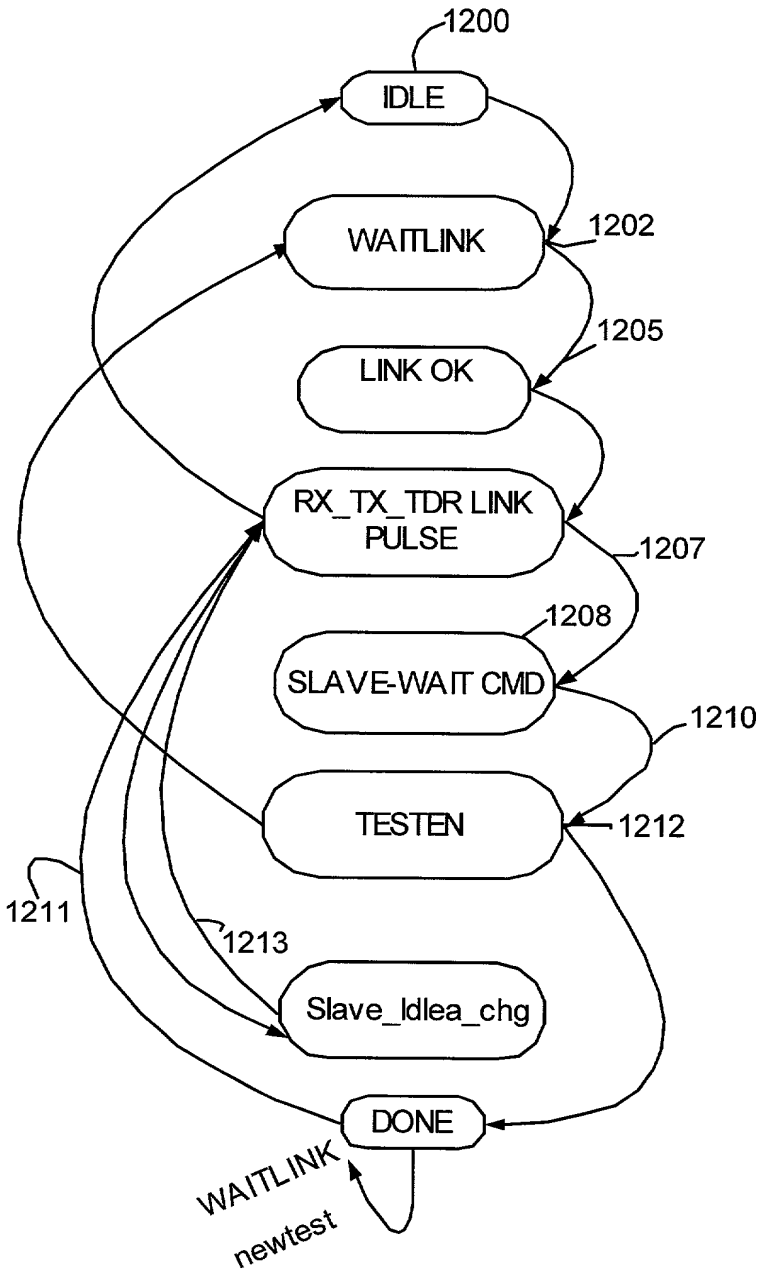


Figure 12

linkdet fsm

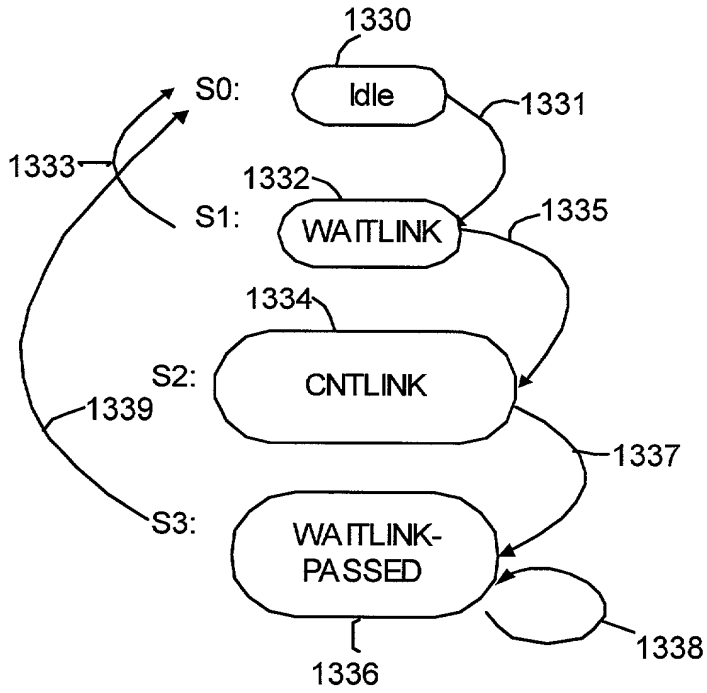
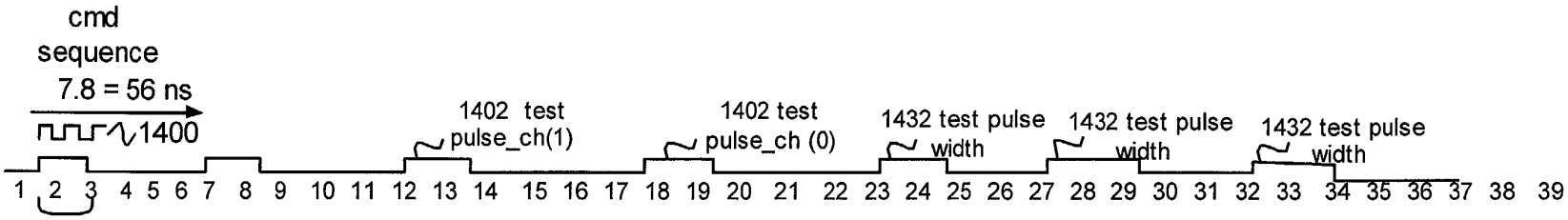


Figure 13

FEXT: and signaling



max # times asserted = 3 T cycles

min # times asserted = 2 T cycles

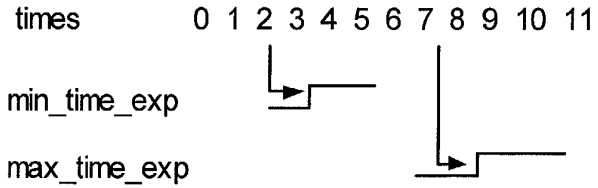


Figure 14

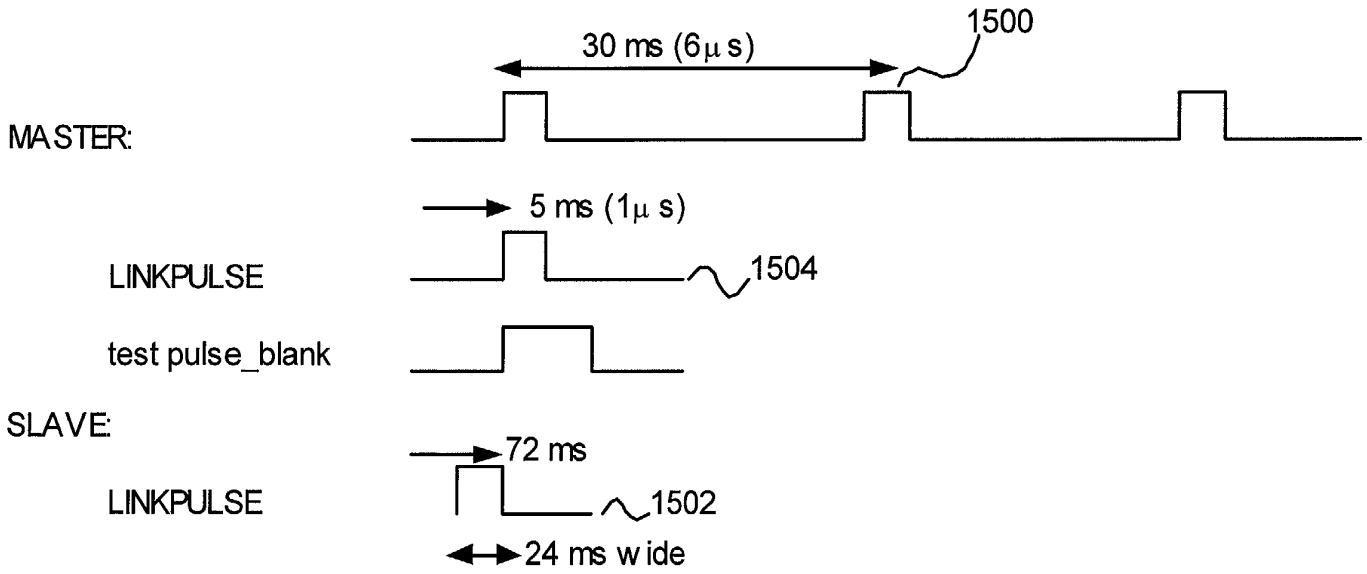

LINKPULSE/TEST PULSE TIMING - NO FEXT
30 ms (6μ s)
1500
MASTER:
5 ms (1μ s)
LINKPULSE
1504
test pulse_blank
SLAVE:
72 ms
LINKPULSE
1502
24 ms w ide

Figure 15

MDIX: Link pulse - no fext

1) No mdix

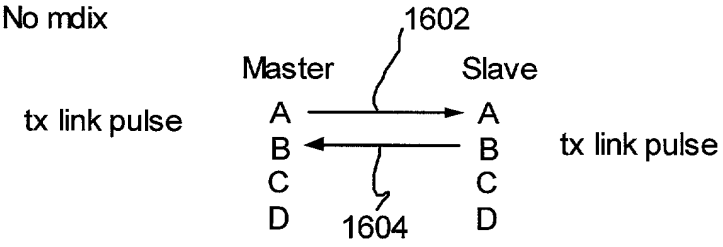


Figure 16A

2) mdix

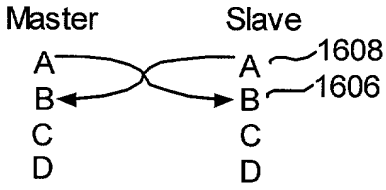


Figure 16B

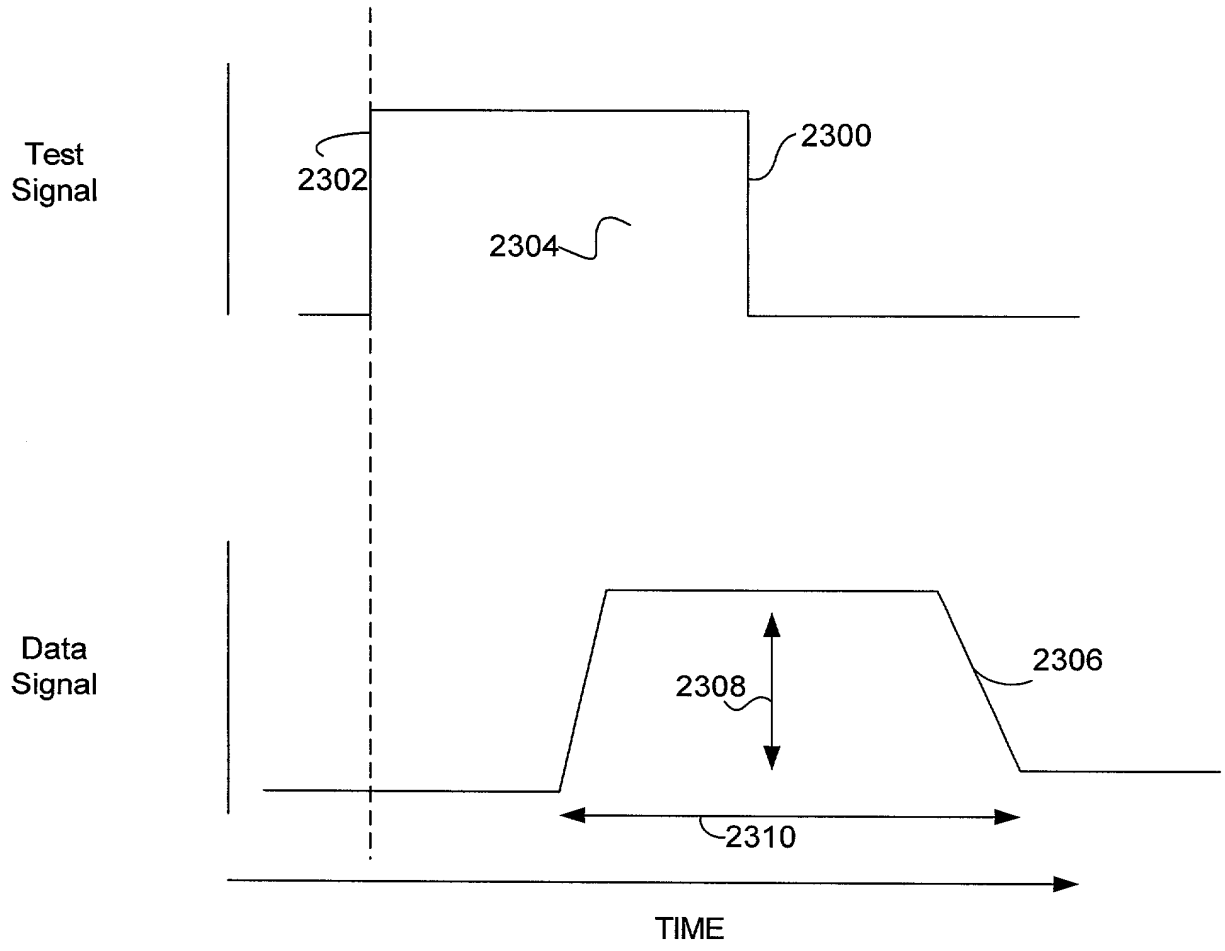


Figure 17

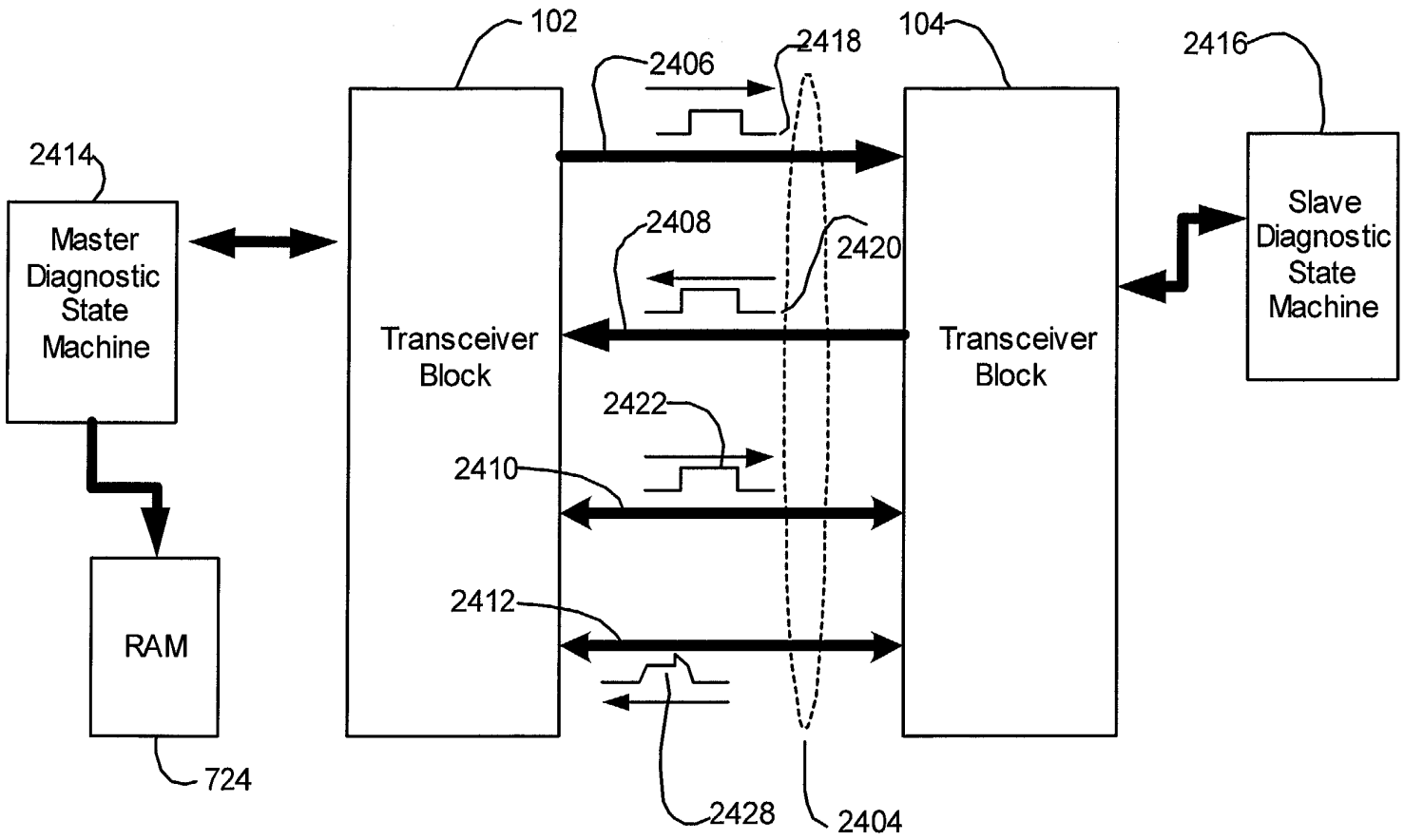

102
104
2406
2418
2416
2414
Master Diagnostic State Machine
Transceiver Block
Transceiver Block
Slave Diagnostic State Machine
2408
2420
2422
2410
2412
RAM
724
2428
2404

Figure 18

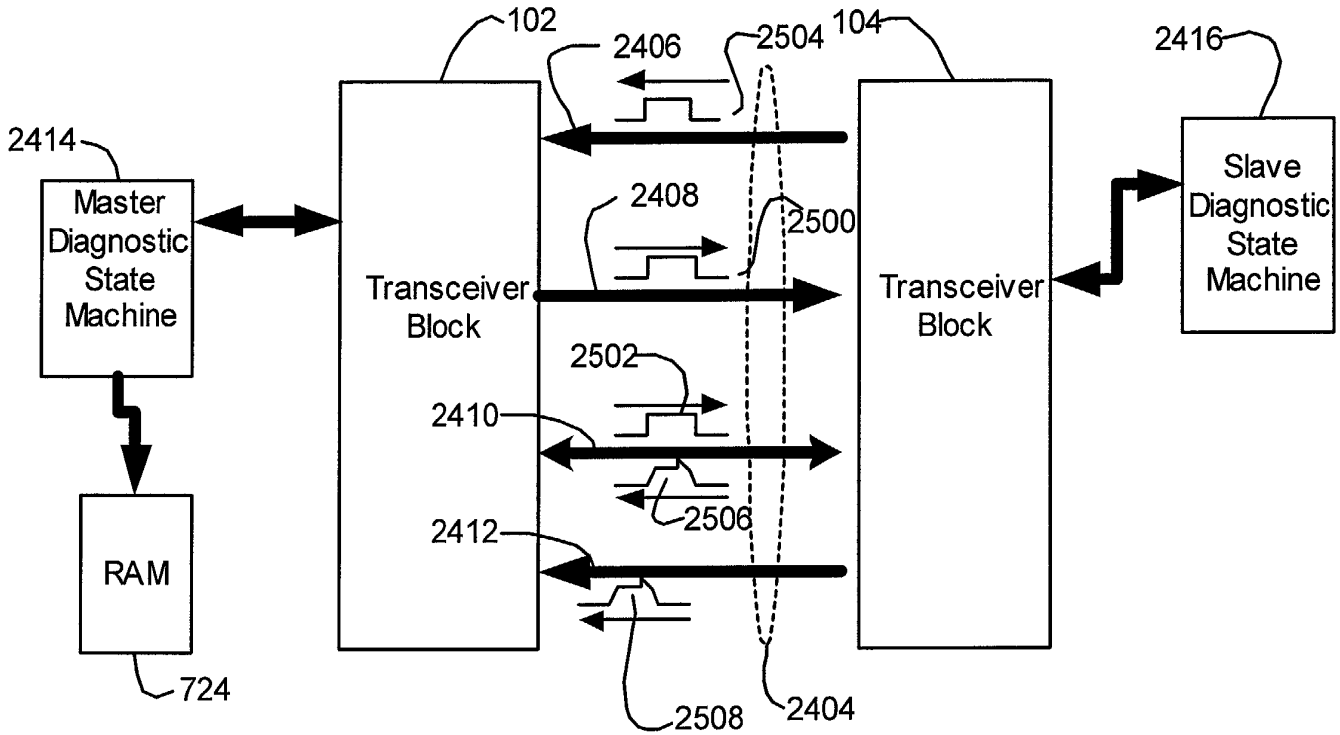

102
2406
2504
104
2416
2414
Master Diagnostic State Machine
2408
2500
Transceiver Block
Transceiver Block
Slave Diagnostic State Machine
2502
2410
2506
2412
RAM
724
2508
2404

Figure 19

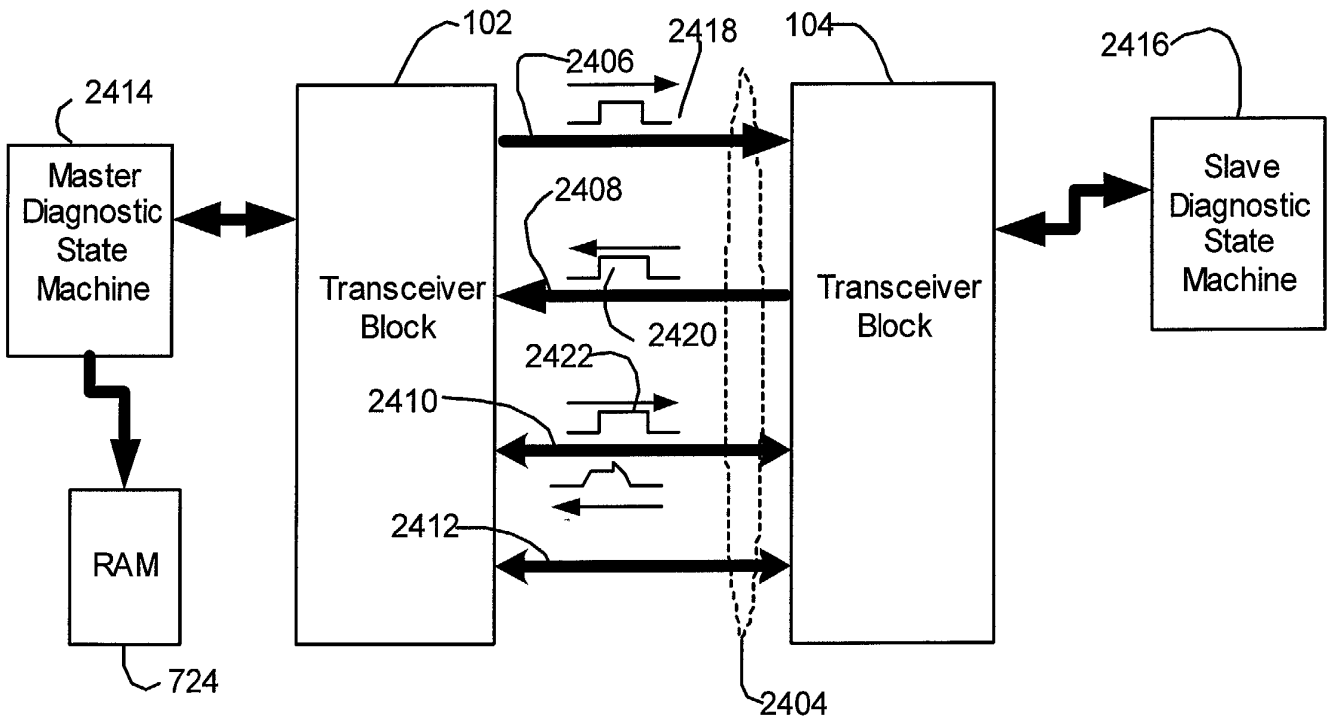

102
2418
104
2406
2416
2414
Master Diagnostic State Machine
2408
Transceiver Block
Transceiver Block
Slave Diagnostic State Machine
2420
2422
2410
2412
RAM
724
2404

Figure 20